Technical Report No. VNIT-RCOEM/R&D/INUP PROJ-IITB/EN2

Fabrication of Micro-cantilever Based Sensor

Principal Investigator: Dr. Rajendra Patrikar

VNIT, Nagpur

Co- Principal Investigator: Mrs. Jayu Kalambe

RCOEM, Nagpur

Research Project at Indian Institute of Technology Bombay under Indian Nanoelectronics User Program (INUP) sponsored by DIT, MCIT Government of India.

Department of Electronics Engineering
Shri Ramdeobaba College of Engineering & Management, Nagpur-440013

2012-13

Contents

1. Introduction 1
2.Microcantilever based sensor with electrical read-out method 2
3.Microcantilever Fabrication 3
3.1. Fabrication of metal cantilever 4
3.1.1 Process details 5
3.2. Fabrication of Polysilicon cantilever 19
3.3 Fabrication of Bi-layer Cantilever 28
4. Electrical characterization 29
4.1 Current-Voltage (I-V) Characterization 31
4.2 Experiments for temperature detection 32
4.3 Transient Analysis of Microcantilever Based Sensor 32
4.4 Experimental Results for single layer and bi-layer cantilevers 34
5. Conclusion 36
References 37
Acknowledgement 38

1. Introduction

One of the most flexible mechanical sensor systems is the microcantilever based sensor. Conventional has the limitation of having high power consumption and sensitivity, Microcantilever technology have the solutions to some of this limitations. The main feature of a cantilever based sensor is transducing the mechanical behaviour of the cantilever into a measurable signal, where the mechanical properties are altered by physical changes in the environment. Microcantilever based sensors have a wide range of applications. Cantilevers have been demonstrated in such applications as gas, temperature, pressure, biological and force sensors. Furthermore, by reducing the dimensions of the sensor to the nanometer scale, the sensor can become faster, cheaper and more sensitive. The microcantilever has become a versatile tool for sensing due to their intrinsic flexibility, together with the availability of techniques designed for monitoring. Differential stress at the surface to the beam of the cantilever causes the bending of cantilever. The cantilever bending can be detected by different read-out methods, such as optical reflection, piezoresistive, interferometric, piezoelectric and capacitive [1-6]. Based on the application one of these methods is chosen for implementation. Most of the detection methods require extra hardware for detection and sensing along with the electronics, hence, the size of the assembly becomes bigger. These methods are costly, require highly sophisticated circuits for measurements and a very precise mechanical alignment or require additional material layers, which is usually difficult in the semiconductor manufacturing. In this work the direct electrical detection is used, which has an advantage of reduced complexity. This readout method is equivalent to ‘hard-contact’ device in which the cantilever is placed close to another electrode. The cantilever is allowed to touch the electrode when the surface stress exceeds the particular limits and current flows through the device indicating the set value of physical parameter under measurement. For most of the applications, desired separation between the electrodes may be less than 50 nm. This small separation is usually required for various sensing application, which is difficult to achieve with existing lithographic and etching techniques. Thus, it is very difficult to obtain and maintain precise gap between the electrodes in nanometers. We have design microcantilever sensor with one micrometer gap between the electrodes, which are easily obtained by existing etching technique. The use of electrostatic actuation is proposed to achieve the desired precise gap between two electrodes.

Our main objective towards this project is to demonstrate the application of Micro-cantilever as a temperature sensor. The design of the device is based on electrostatic actuation of a vertically deflecting cantilever and the readout method employed is electrical i.e current is used to detect the temperature. This readout method is based on measuring current change at the cantilever beam and a static parallel electrode contact interface. On the verge of the same, the differential stress developed due to change in temperature resulting in nano mechanical deflection is sensed. We have fabricated single layer Aluminium, Polysilicon and bi-layer cantilever (Polysilicon-Gold) and thorough electrical characterization of these sensors was done to verify the functionality of the sensor.

2. Microcantilever based sensor with electrical read-out method

Microcantilever have got potential applications in every field of science ranging from physical and chemical sensing to biological disease diagnosis. The sensing action essentially is the deflection of the cantilever beam. Deflection of microcantilever sensor is in nanometers in response to surface stress developed due to change in physical parameter like temperature and biological entities. Measuring such small deflection is always a challenge. Therefore many read-out methods described in the literature fabricate extra hardware elements to measure such gap such as LASER, layers of piezoresistive or piezoelectric materials. The fabrication process thus becomes costly and complicated since these materials or elements are not routinely used in CMOS technology. In this work we have developed simpler electrical detection method which does not need such additional components. The cantilever is working under the driving voltage as well as the external physical parameters. Design of microcantilever with new readout method developed is shown in Fig. 1.

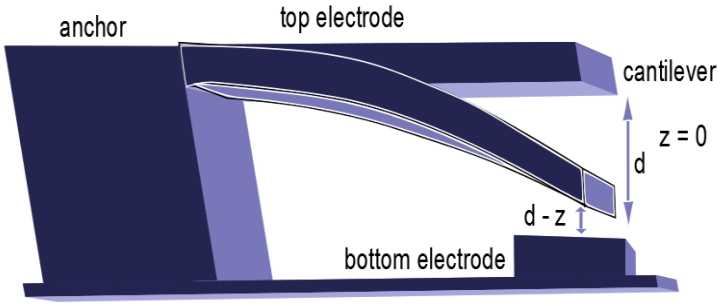


Fig. 1. Microcantilever based sensor with bottom electrode

In the proposed method the contact pad with metal is fabricated below the cantilever tip. Due to the deflection the cantilever tip will rest on this pad and electrical short is created. The cantilever is allowed to touch the electrode when the surface stress exceeds the particular limits. When cantilever is in contact with bottom electrode current starts flowing through the electrode which detects the physical parameter under measurement. This method is equivalent to digital read-out method, i.e. current flows if the physical parameter exceeds particular limit.

3. Microcantilever Fabrication

Developed method is validated with experiments performed on fabricated microcantilevers. Fabrication process is complex and crucial which involve mainly three processing steps- film deposition, lithography followed by etching. Fabrication process technologies are described in [7-9]. The process to fabricate the microcantilever using surface micromachining process has been developed which involves five level lithography processes. The schematic of generalize fabrication process for microcantilever using surface micromachining is shown in Fig.2. Different methods were tried to remove the sacrificial layer which is challenging. Optimization in this regard has been done and finally the microcantilevers were successfully released. Single layer metal, Polysilicon, and bi-layer microcantilever devices have been successfully fabricated after optimizing the process parameters. The fabrication and characterization facilities available at IIT, Bombay are avail under INUP Program [10].

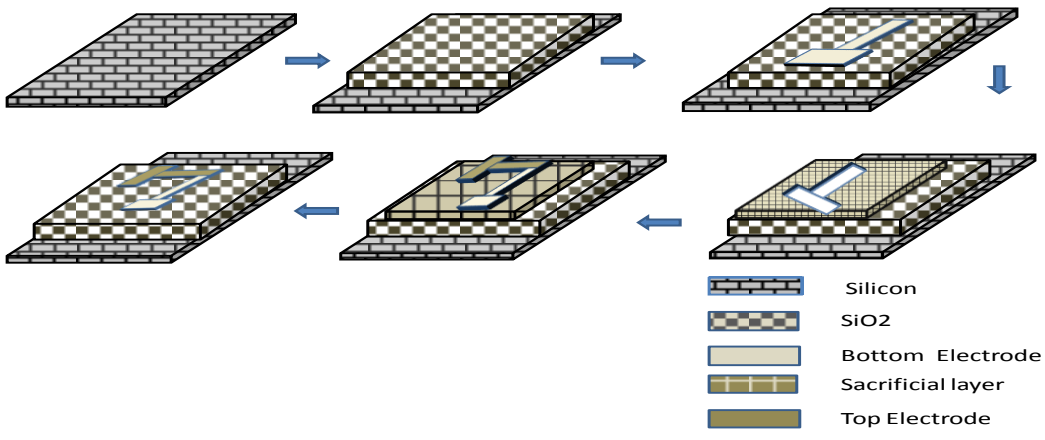


Fig.2. Schematic of generalize fabrication process for microcantilever

3.1. Fabrication of metal cantilever

Fabrication process incorporates five different photo masking levels. Fabrication process performed on high resistivity p-type <100> silicon wafer begins with the deposition of an isolation layer on top of the silicon substrate using thermal oxidation process. Aluminium is used as structural material for cantilever as well as for the bottom electrode and is deposited using thermal evaporation process. In this fabrication process bottom electrode is formed first. Next, sacrificial layer (PPR) is deposited on top of the bottom electrode and patterned. This step is followed by the deposition and patterning of a 0.5 μm thick Aluminium layer to create the cantilever beam. Finally the cantilevers were released by removing the resist.

3.1.1 Fabrication process details

The Aluminium cantilever sensor is fabricated & the process related issues are studied. Fabrication process developed is shown in Fig. 3.

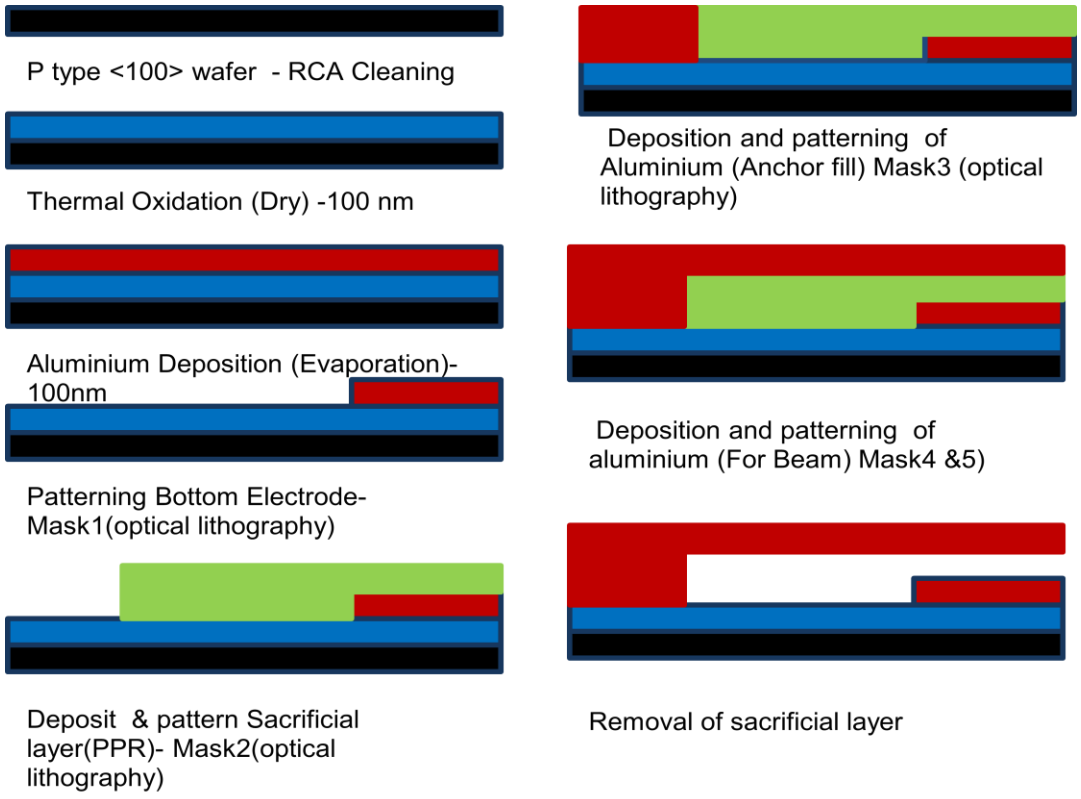


Fig.3. Schematic stepwise process flow for Aluminium cantilevers

Mask used in lithography process is shown in Fig. 4.

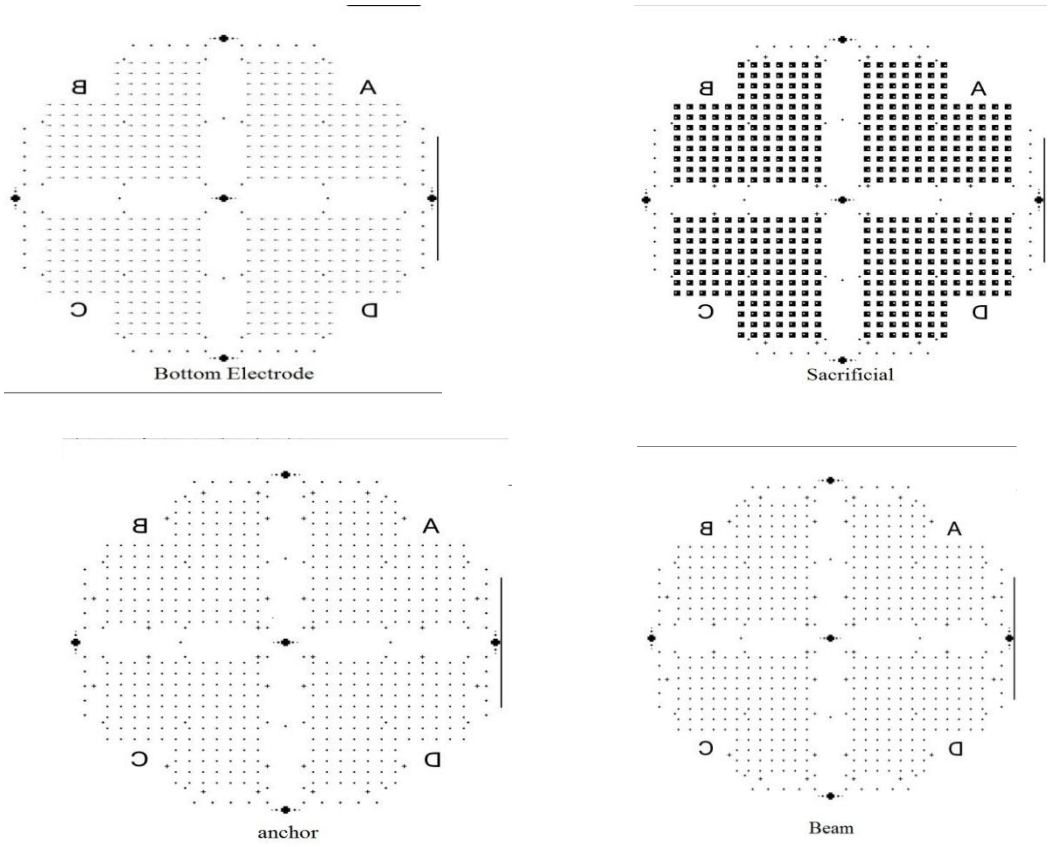


Fig.4. Mask design for various masking level.

3.1.1 Process details

P type wafer <100> orientation of high resistivity which allows the possibility for integration with CMOS for multifunction assemblies say more than 10Ωcm is used for fabrication.

1) Wafer cleaning→ Radio Corporation of America (RCA) cleaning has been done to remove the contaminants from wafer. RCA removes organic contaminants (such as dust particles, grease or silica gel) from the wafer surface; then removes any oxide layer that might have built up and finally, removes any ionic or heavy metal contaminants. It is a standard set of wafer cleaning steps which needs to be performed before any high temperature process. RCA cleaning is a two steps process:

SC 1 - standard clean 1 is done to remove organic contaminants. After SC 1, HF dip is given to the wafer to remove the oxide layer that might have been formed during this process.

SC 2 - standard clean 2 is done to remove the traces of metallic contaminants.

SC 1 → 180 ml DI water + 25 ml NH_4OH at 70°C, 5min
Add 50 ml H_2O_2 and heat for 6 - 8 min
Allow wafer to cool for 10 - 20 min
DI water dip, 30 sec HF dip, DI dip

SC 2→ 180 ml DI water + 25 ml HCl at 70°C for 5 min
Add 50 ml H_2O_2 and heat for 3 - 6 min
Allow it to cool for 10 - 12 min
DI water dip, 30 sec HF dip, DI dip.

RCA cleaning wet bench is shown in Fig. 5.

RCA cleaning bench:

- RCA chemicals used: DI water, NH_4OH, H_2O_2, HCl, HF
- Piranha chemicals used: H_2SO_4, H_2O_2
- HF cleaning: 2%HF
- Substrates used: Si, glass.
- Substrate size: Max 4" diameter wafer.

Fig. 5. RCA cleaning wet bench

2) Thermal oxidation (SiO_2)

Oxidation of the wafer is done to improve isolation between devices and provide protection against any implant and diffusion. An oxide layer of 100 nm has been grown over RCA cleaned silicon wafer using thermal oxidation process. Oxidation of silicon slice can be carried out by subjecting it to oxygen or water vapour, while it is maintained at elevated temperature.

Process recipe:

- SiO_2 thickness - 100 nm
- Wafer temperature - 1100°C
- Time - 45 min

Furnace 2 is used for thermal oxidation shown in Fig.6.

Furnaces 2:

- **All tubes can handle 2 inch wafers**
- **Pyrogenic oxidation furnace** - Temperature up to 1150^0 C – gases H_2 and O_2
- **Double walled furnaces**: Uniform growth of oxide – only dry oxidation of silicon wafers
- Solid source dopant and spin on dopant. Max. temp. is 110^0C, gases used: O2, H2 & N2

Fig. 6. Furnace 2

3) 1st level Aluminium deposition.

Process recipe:

- Thickness: 100 nm.
- Metal weight: ~100mg.
- Chamber pressure: 4.3 x 10^{-6} torr.
- Flash Deposition technique employed.

Thermal evaporator is used for aluminium deposition shown in Fig.7.

Thermal Evaporator:

- **Wafer size:** 2 Inch at a time 2-3 wafers can be processed if required
- **Number of current sources to head the filament:** two
- **Number of filaments that can be fitted in the system:** two
- **Material:** Al
- **Base pressure**: 8 X 10-5 mbar
- **Substrate temperature**: Room temperature
- **Coolant required**: Liquid Nitrogen
- **Additional facility**: Shadow masks of 1mm diameter available for making MOS capacitors.

Fig.7. Thermal Evaporator

4) 1st level of Aluminium patterning is done to create a bottom electrode with contact as shown in Fig. 8.

Photolithography is done to pattern the layers of the device. It is process of transferring geometric shapes/patters on a mask to the surface of silicon wafer. It uses optical properties of photosensitive materials to transfer patterns on the desired surface.

Process recipe:

- Dehydrate - 110°C for 30 mins.
- PPR coating - 500 rpm for 10 sec, 3000 rpm for 30 sec
- Prebake (soft bake) - 90°C for 2 min
- Mask alignment.
- Exposure – 7-8 sec UV exposure.
- Development – MF319, 30 to 45 sec.
- Post Prebake (hard bake) - 90°C for 2 min
- Removal of unexposed PPR by Acetone after etching.

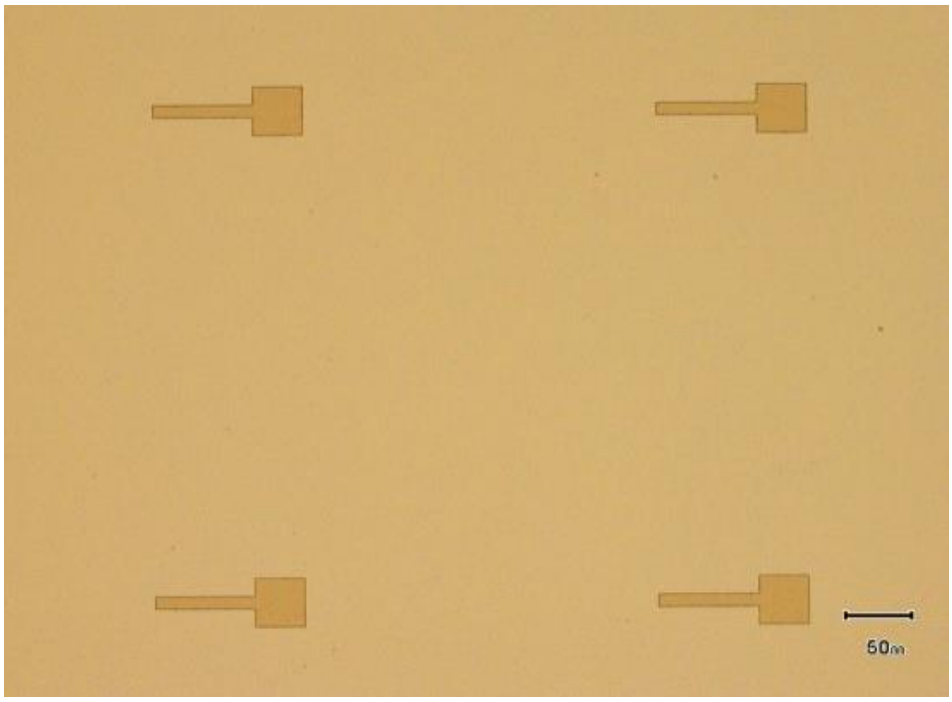


Fig. 8. 1st level of Al patterning

For lithography used in Double Sided mask Aligner is used shown in Fig. 9.

Specifications of the system:

- **Exposure modes:** hard, soft, vacuum contact
- **Separation distance:** 0-300 microns
- **Wafer thickness**: 0.1-10 mm
- **Lamp:** 500W Hg Lamp
- **Wavelength range**: 350-450 nm
- **Alignment accuracy:** 0.5 micron for top side and 1 micron for bottom side
- **Minimum feature size achievable:** 2 micron

Process Capabilities:

- **Substrates used**: Silicon, glass
- **Mask plate size:** 3”, 5”
- **Substrate size**: 2”, 4”, quarter of a 2” wafer
- **Gases used**: GN2
- **Positive resist used**:

Fig.9. Double Sided mask Aligner (DSA)

5) 1st level Aluminium Etching. (Wet etching)

Etchant : Aluminium etchant (Phosphoric acid + Acetic acid + Nitric acid+ DI water)

- Used composition:

160 ml H3PO4 + 10 ml CH3COOH + 10 mlHNO3 + 20 ml DI water.
Etch Rate: 100nm in 2-3 mins.

6) 2nd level Resist spinning.

Process recipe:

> Dehydrate 110°C for 25-30 mins.

> Drop cast resist S1813.

> spin at a) 500 rpm for 15sec

b) 6000 rpm for 30sec or 4000 rpm for 50 sec.

>Resist thickness = 1 micron.

Spinner used for resist spinning is shown in Fig.10.

Spinner:

- Substrates that can be handled – Silicon, glass, any other substrate
- Substrate size – 2", 4", 6"and 8" wafers and quarter of a 2" wafer.

Maximum speed – 6000 rpm

Fig.10. Spinner

7) 2nd level PPR Patterning is done to create cavity for anchor as shown in Fig.11.

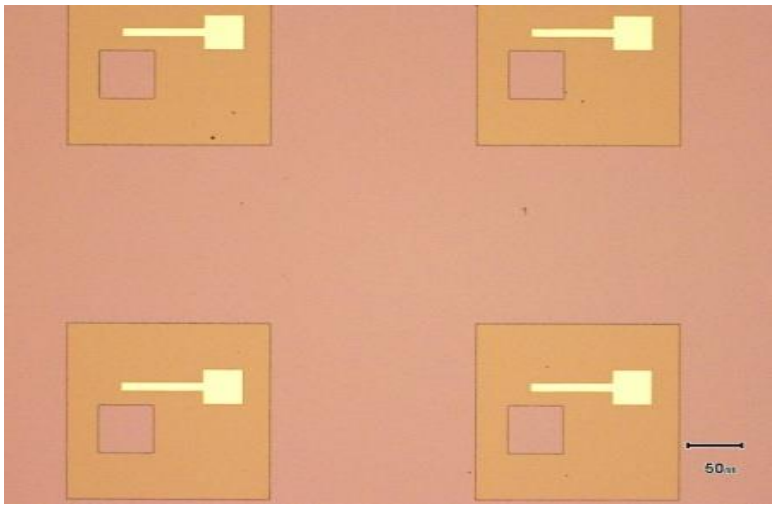


Fig. 11. 2nd level of S1813 resists patterning

8) 3rd level of Aluminium deposition:

Process recipe:

- Thickness: 800 nm.
- Metal weight: ~400 mg.
- Chamber pressure: 4.3 x 10^{-6} mtorr.
- Flash Deposition technique employed.
- Thickness obtained: 855nm (Measurement using Surface Profilometer).

9) 3rd level of Aluminium Patterning is done to create anchor (same is used as contact) as shown below in Fig. 12. (Same recipe is used but, this time the samples were not dehydrated)

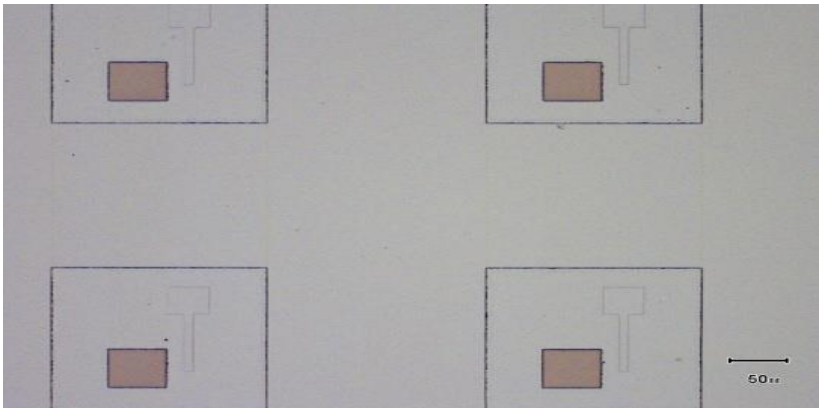


Fig. 12. 3rd level of Al patterning

10) 3rd level of Aluminium Etching (Wet etching)

- Used composition:

160 ml H3PO4 + 10 ml CH3COOH + 10 mlHNO3 + 20 ml DI water.

11) 4th level exposure is done to remove the resist over 3rd level patterns as shown in Fig.13.

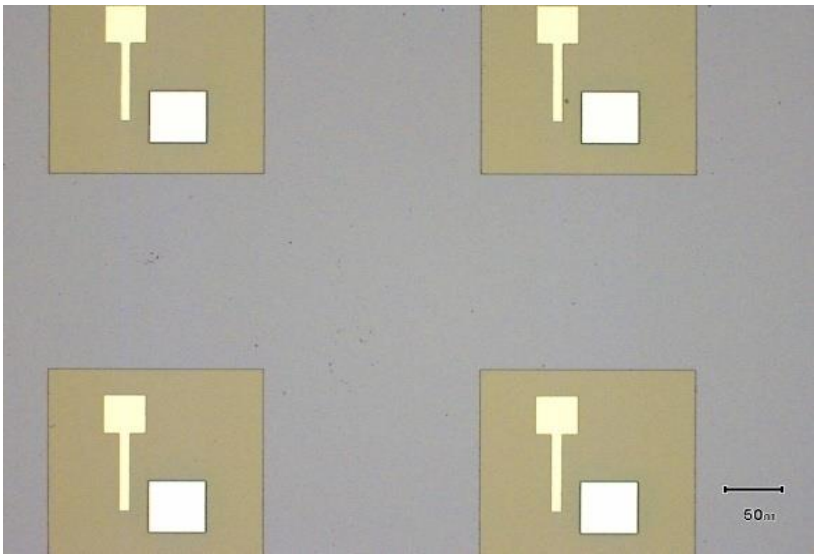


Fig 13. 4th level UV Exposure and development.

12) 4th level exposure followed by immediate 5th level Al deposition and 5th level patterning is done to transfer a beam structure to layer through mask and etching as shown in Fig. 14.

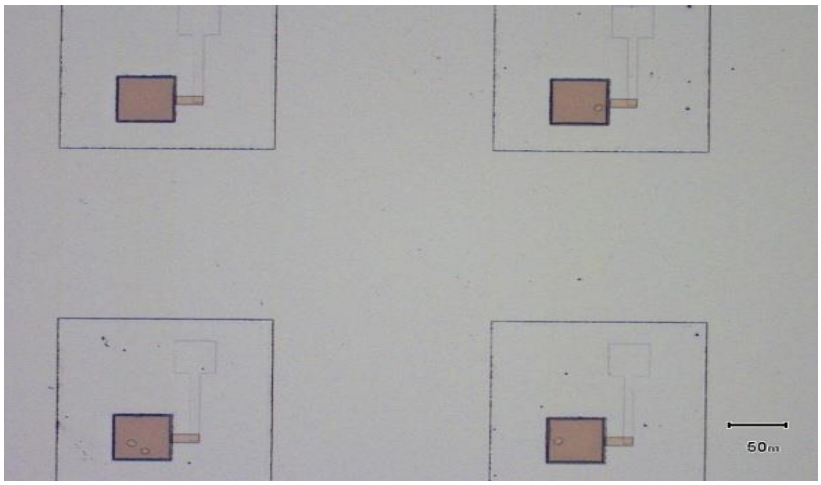


Fig 14. 5th level Al Patterning

13) Removal of Sacrificial Layer.

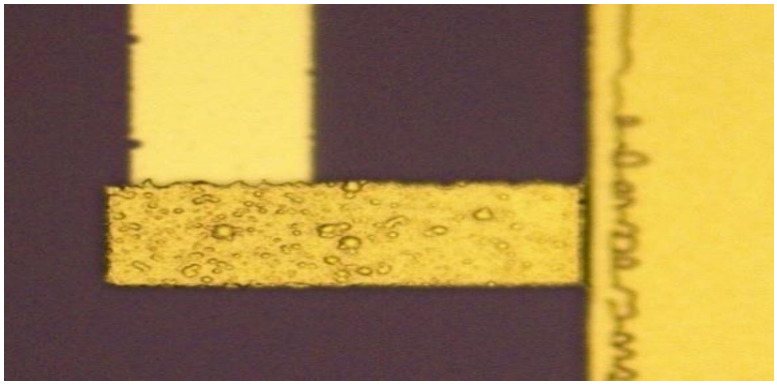
The various releasing techniques are employed to remove the resist (sacrificial layer) are

1) RF O_2 Plasma ashing.
2) Acetone Dip
3) Microposit remover.
4) Evaporation.

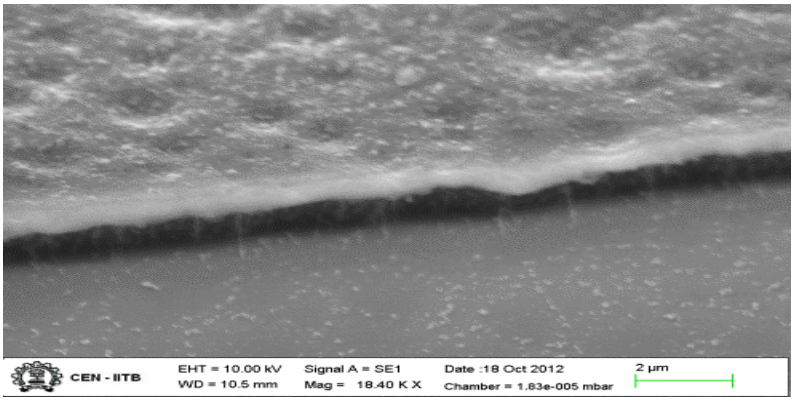
i) RF O_2 plasma ashing is done for different RF power, gas pressure and time duration, but a very long duration of ashing was required which could lead to deformations in aluminium beam when exposed to plasma for a long duration of time.

Fig.15 a) shows the beam surface is eroded with longer duration ashing.

Fig. 15 b) show the SEM image of the RF ashing done and resist is still not removed.



(a)

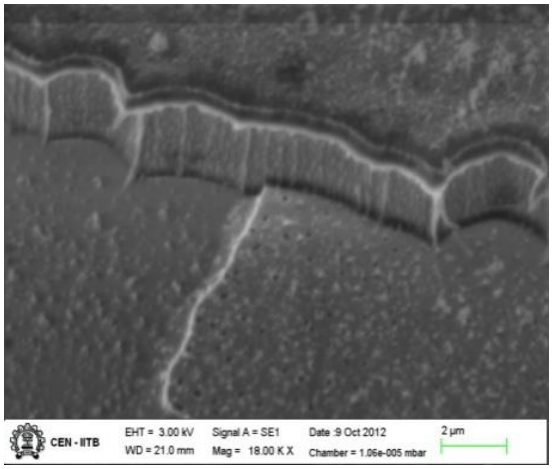


(b)

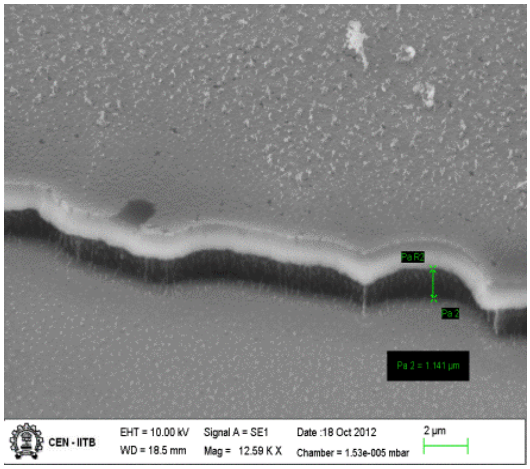
Fig, 15. Images of microcantilever after plasma ashing (a) Surface Image (b) SEM Image

Fig.15. show that the RF ashing was done for different RF power and time, still the resist underneath is not removed. Even for doing it for more than an hour, the resist persist.

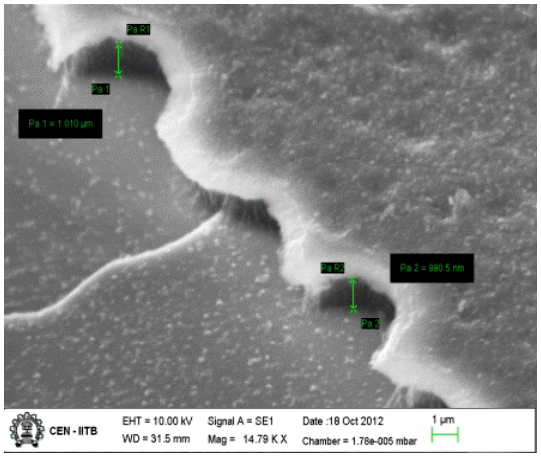
ii) Again the plasma ashing is done with some inclination is given to the sample to help plasma to reach underneath. 100 watts for 35mins is enough for ashing 1 micron resist. But for the resist underneath the beam need more time for ashing, nearly 45^0 tilt was provided to the samples inside the ashing chamber, 100 watts for 40 mins. It was found that it is still difficult to removed most of the resist. Experiments will be done once more with higher inclination and more ashing time. Ashing was done at 100 watts 40 mins, it can be seen clearly that most of the resist except that underneath the beam is not removed



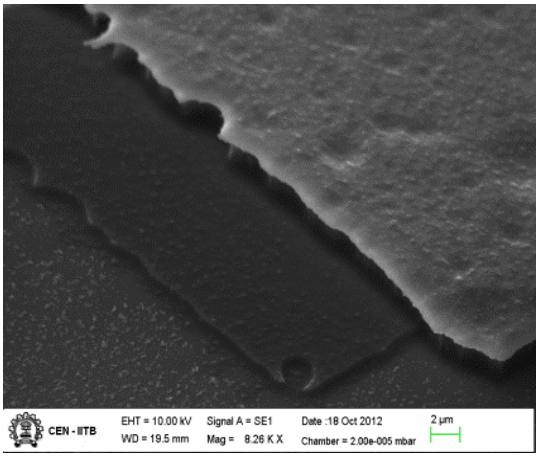
a) 80watts, 50sec



b) 100watts, 10mins



c) 100watts, 15mins.



d) 100watts, 30 mins

Fig. 16. Plasma ashing at different watts and time period

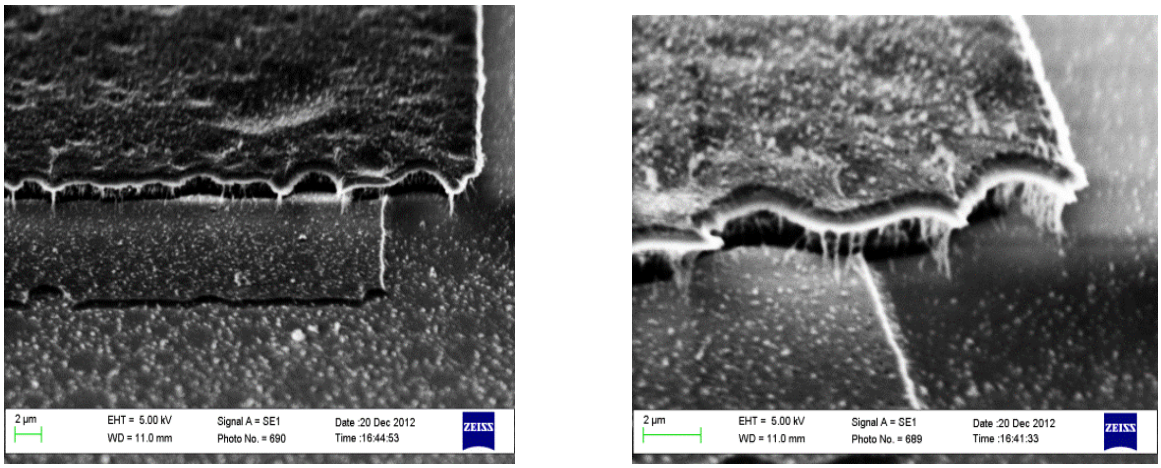


Fig.17. Ashing was done at 100 watts 40 mins

iii) RF ashing was done by giving tilt or inclination of about 45 °C, it shows that the beam is also sputtering a little at edges.

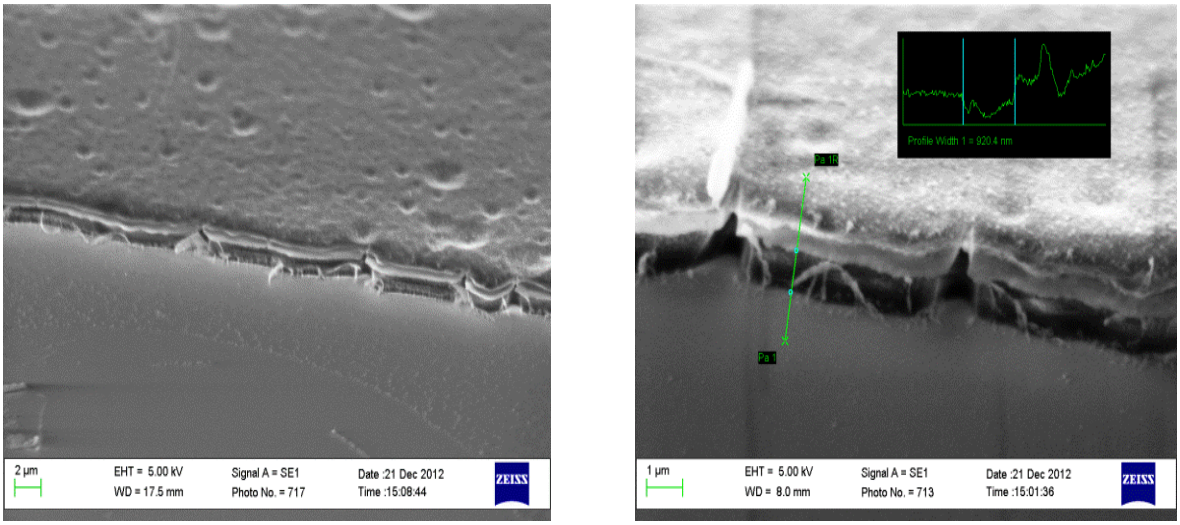
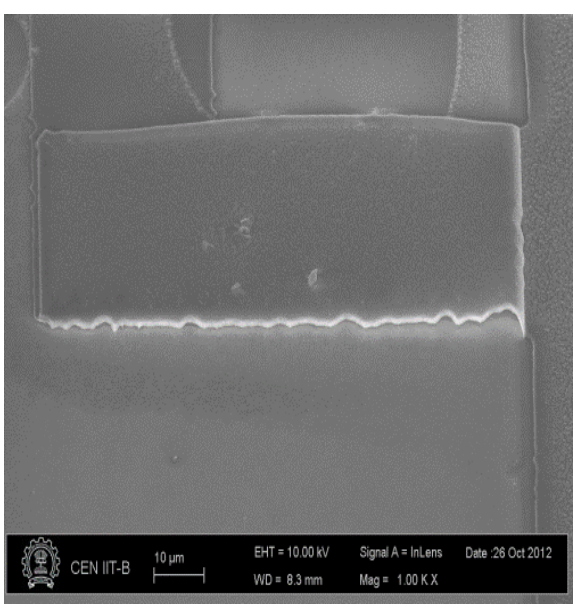
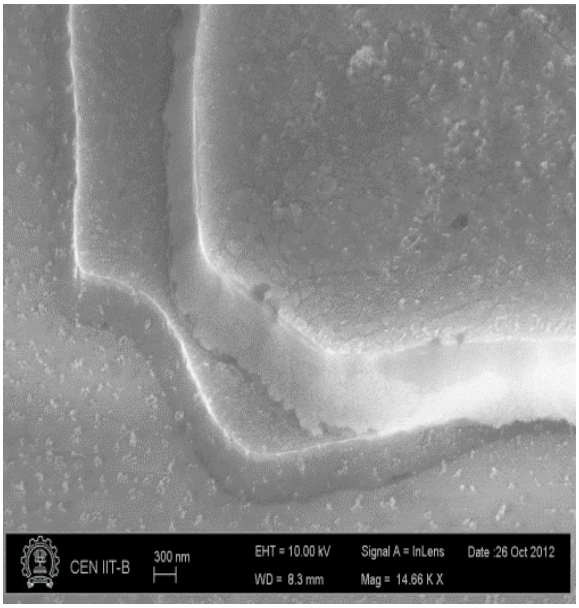


Fig.18. Plasma Ashing with inclination of sample at 45^0

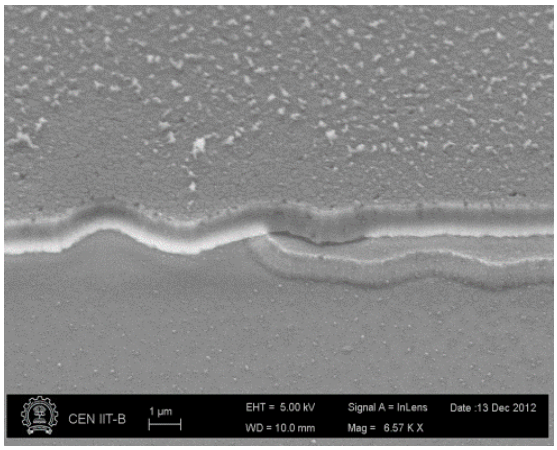
For the second case, Acetone dip was performed overnight and was found that the beam stick to the bottom electrode due to stiction /adhesion and was found same with the third case. i.e microposit remover 1600 which is specially used for PPR removal.



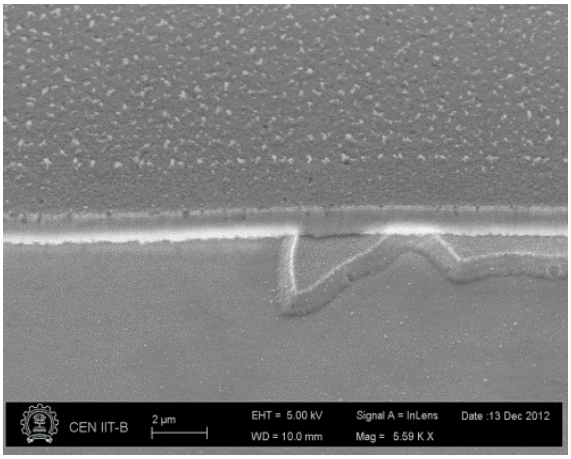
(a)



(b)



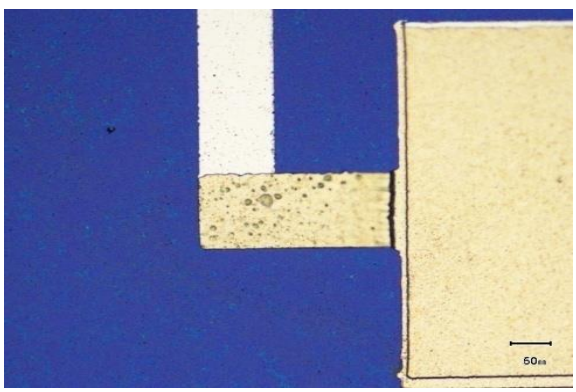
(c)



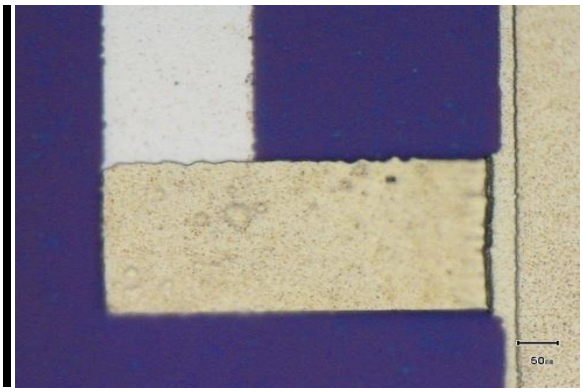
(d)

Fig.19. SEM image that show that the beam is suspended but stick to the bottom electrode

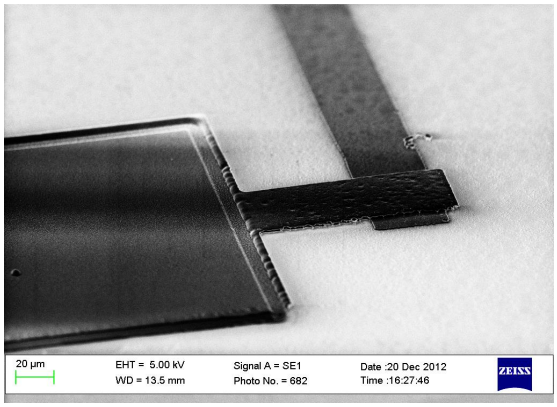
Finally the cantilevers were released by stripping the resist in Acetone and evaporating the Acetone at room temperature (i.e. 21^0C).



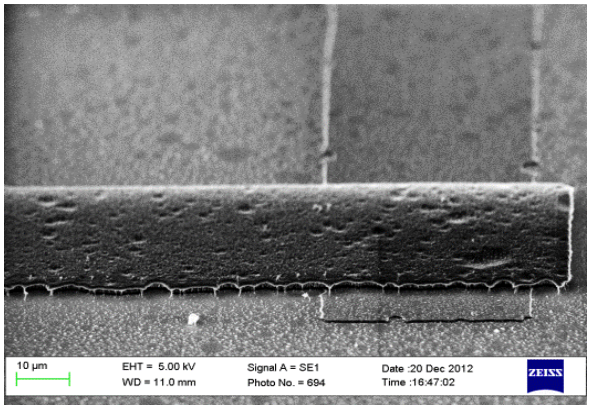
(a)



(b)



(a)



(d)

Fig.20. shows the resist was removed after evaporation of Acetone

With respect to fabrication processes carried out to achieve proposed microcantilever sensor a better and a deeper outlook was observed with respect to fabrication issues faced and methods deployed to overcome those issues. We are able to study the different methods of releasing the cantilever device and finally we concluded that the best feasible option is that of Evaporation of Acetone. Microcantilever is successfully fabricated and photograph of device is shown in Fig.21.

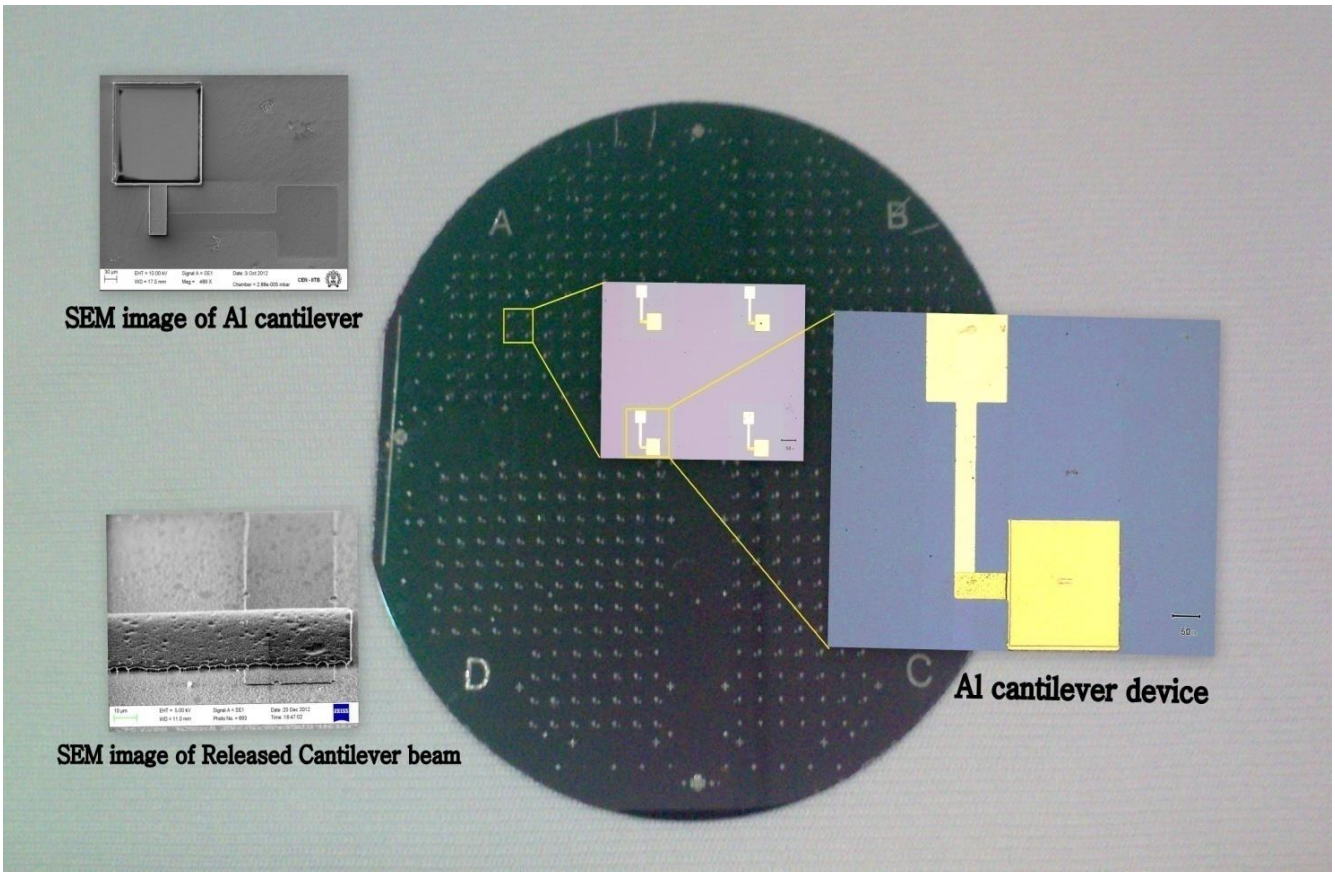


Fig. 21. Photograph of Fabricated microcantilevers after optimization process

3.2. Fabrication of Polysilicon cantilever

We have also fabricated single layer and bi-layer Polysilicon cantilevers, since it has the lowest thermal expansion coefficient and it is IC Compatible. For bi-layer structure, gold was deposited on polysilicon to make it a bi-layer. The fabrication process is discussed below.

Micro-cantilever is designed on single sided p type <100> silicon wafer with high resistivity. The device design steps starts with the selection of Silicon substrate followed by deposition of a silicon dioxide (SiO_2) using thermal oxidation. Insulating layer on the silicon substrate is followed by the deposition and patterning of a doped polysilicon layer deposited using HWCVD method that works as the bottom electrode. Next, on top of the polysilicon layer, sacrificial SiO2 layer is deposited using ICPCVD method and patterning is done. This step is followed by the deposition and patterning of a 0.5μm thick polysilicon to create the top layer of the cantilever beam. Polysilicon is used as the structural material and silicon dioxide is used as sacrificial layer.

The device has been released with wet etching method using BHF. Optimization regarding the release fabrication process of microcantilever has been done.

3.2.1 Fabrication process details

1) Wafer cleaning: process details are discussed in section 2.1

2) Thermal oxidation (SiO_2) : process details are discussed in section 2.1

Recipe:

SiO2 thickness - 250 nm

Wafer temperature - 1100°C

Time – 2hrs 15 mins

3) Polysilicon deposition. (Using HWCVD):

HWCVD is a new technique which is used to deposit thin layer of polycrystalline silicon on substrate. In HWCVD the reactant gases Silane, diborane and hydrogen (reactant gases) thermally decomposed at the surface of resistively heated filament whose temperature is in range of 1500-2000 ^oC to form radical. These radicals then form other species and get deposited on the substrate whose temperature range is 0 to 800^oC. In HWCVD the deposition rate is governed by filament temperature and flow of gases. Base pressure for deposition should be in range of e^{-6} or e^{-7} mbar.Initially we set the base pressure which was 5.5 e^{-7} then, we set the substrate temperature which was 300 ^oC since the substrate affects the deposition rate and quality of film so we kept the temperature 300 ^oC which was fine with our device. After setting the substrate temperature we set the ratio of gases which was SiH4:B2H6:H2 in the ratio of 1:5:10 using set point in the gas flow controller and gas pressure was set which was $2.6e^{-1}$ m bar. Once the gas pressure set there would be actual flow of gases in the desired ratio. After that we set the filament temperature to 1850 ^oC. The filament temperature was kept 1850 ^oC since at sufficiently high temperature only the silane SiH_4 is fully cracked into one si and four hydrogen atoms. Also at about 1800 ^oC maximum production of si atoms was observed. The main issue with HWCVD is the control of substrate temperature and aging of filament which needs to be controlled. With HWCVD, it is possible to deposit multi layers of polysilicon. As there is no ion bombardment in HWCVD also its cost is low and has higher deposition rate than PECVD. Initially, for the bottom electrode the deposition was done for 30mins and the thickness was checked in Surface profile

which was around 250nm. Next time when we again did deposition with same recipe and process parameters for 30mins the thickness obtained was around 700nm (CROSS SEM in Raith 150) which was due to replacement of gas regulator. Again we run the process with same recipe and process parameters for 1 hour and measured the thickness in Raith 150 by doing CROSS SEM and it was around 1 micron which was desired for our structure. It was observed that thickness of 500nm was difficult to get since for 30mins the thickness was 700nm and for 20mins it was 250nm so we had to compromise and did the deposition for 30mins (700nm around). Actual wafer loaded inside the chamber of HWCVD at room temperate and recipe used is as follows:

Base pressure=1.7e-6

Gas pressure=1.1e-1

Substrate temperature=300degree celsius

Filament temperature=1850 degree celsius

Ratio of gases SiH4:B2H6:H2=1:5:10

Voltage=22.7volts and Current=13.7Amp

Process time=30 minutes

SEM image is taken after polysilicon deposition shown in Fig.22.

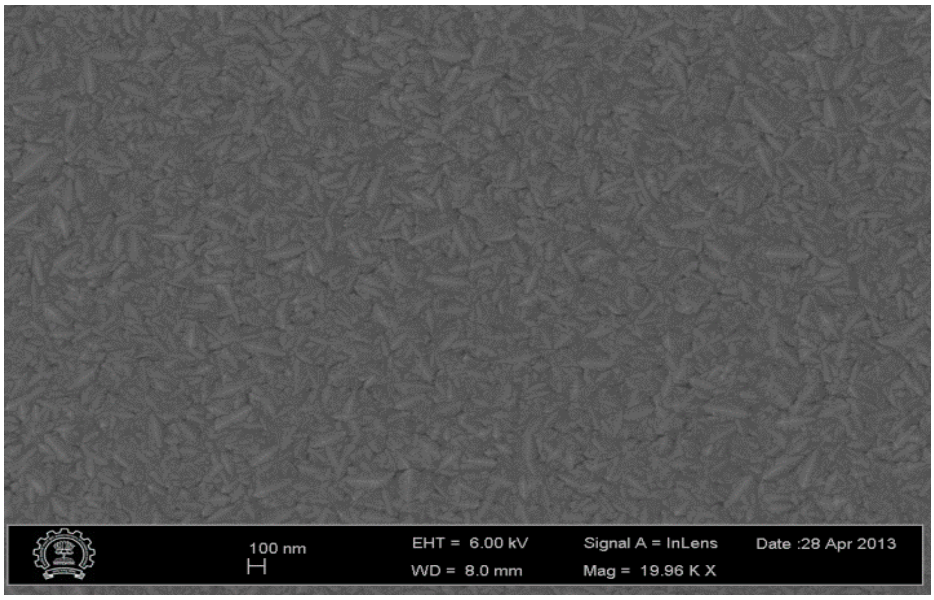


Fig 22. SEM image: Surface topography of HWCVD deposited polysilicon

Polysilicon is deposited using hot wire CVD device shown in Fig. 23

HWCVD:

- ***Make and Model:*** *The system was designed and assembled at IIT Bombay*
- ***Process Capabilities:***
- ***Substrate Size:*** *2 Inches, small pieces of wafer- Si and glass.*
- ***Type of depositions:*** *intrinsic polysilicon, Boron doped polysilicon, silicon nitride.*
- ***Substrate Temperature:*** *Room temperature to 800°c.*
- ***Filament Temperature:*** *Up to 2000 °C.*
- ***Process Gases used****: Silane (SiH4), Ammonia (NH3), Hydrogen (H2), Diborane (B2H6), Nitrogen (N2).*
- ***Chamber Base Pressure****: Up to 10e-7 mbar.*
- ***History of the substrate:*** *Silicon wafers, Glass substrate, wafers coated with SU8, oxide deposited wafers.*

Fig.23. HWCVD System

4) Lithography and RIE of polysilicon

After deposition of polysilicon the 1st level lithography was done to transfer the pattern for bottom electrode on full wafer. After that dry etching was done in STS RIE for removing polysilicon from unwanted region. The recipe used for etching polysilicon is as follows:

Recipe:

Gases used SF6=25 sccm,

Chamber Pressure = 100 mtorr

RF Power= 150 watts

Etching time= 30 seconds

In order to verify the etching time, polysilicon was etched and checked in Ellipsometer .

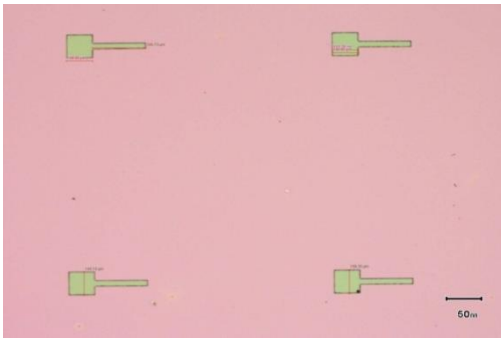


Fig 24. 1st level masking for bottom electrode

5) Deposition and patterning of Oxide with ICPVD .

ICPCVD is as plasma enhanced chemical vapour deposition using inductively coupled plasma as the source. With ICPCVD it is possible to deposit dense film with substrate temperature in the range of 0 to 400^{o}C where as in case of PECVD to achieve high dense film the system uses temperature greater than 400 ^{o}C which can damage the substrate. ICPCVD is a non conformal uniform deposition technique.

Initially the chamber was cleaned using CF_4 and O_2 then gases were allowed to flow through MFC (Mass flow controller) as per the mentioned recipe. The recipe used for deposition of 1 micron oxide was silane SiH_4 16 sccm, N_2O = 40 sccm and process parameters were process

temperature=250 ^{o}C to achieve dense film, Chamber pressure = 20 mtorr, RF power=30 watts and ICPRF=1000 watts. And deposition time was 16 mins for 1micron deposition.

Initially the chamber was cleaned using CF4 and O2 then wafer was loaded inside the chamber.

The recipe used for deposition is as follows:

Gases used: SiH_4=16 sccm

N_20= 40 sccm

Temperature=250 ^{o}C

Chamber pressure=20 m torr

RF Power= 30 watts

ICP Power=1000 watts

Deposition time=16 minutes

Deposited oxide thickness=1 micron

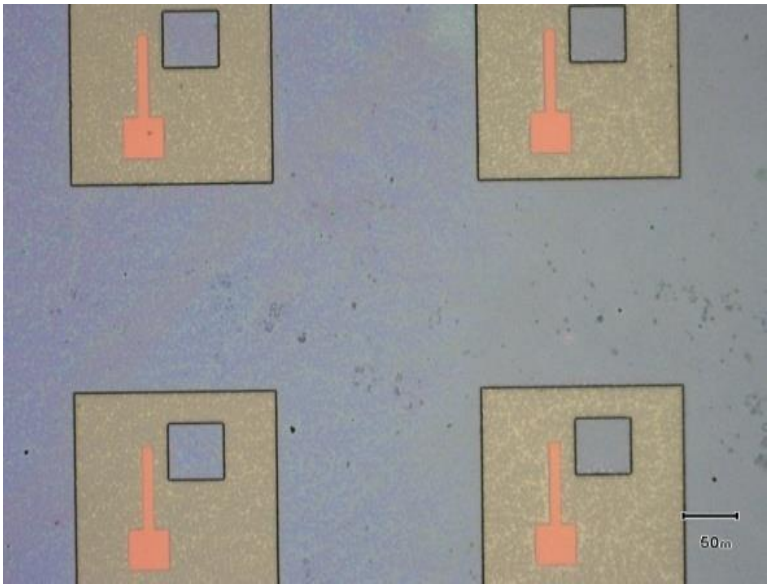


Fig 25. 2nd level anchor patterning after wet etching

After deposition of 1 micron oxide, patterning was for done for 2^{nd} level to create anchor post. PPR with HMDS was used for patterning as PPR and Sio_2 adhesion is poor so HMDS was used for adhesion purpose. For etching 1 micron oxide various methods was tried. Initially it was tried with wet etching using BHF 5:1. It was found that etch rate was very less 30 seconds for 1micrometer it was difficult to control as Teflon tweezers were needed to be used. Also the wet etching was isotropic i.e equal in all directions. Along with vertical etching, lateral etching also occurs which was difficult to control. After that etching of 1 micron oxide was tried in STS RIE and the recipe used was CHF3=20 sccm, O2=1 sccm, Pressure=20 mtorr, Power=400 watts. Initially in STS RIE the etching was tried for 10 minutes and found that in 10 minutes it etched 200nm only again the same recipe was done for 20 minutes but found that the system was unable to etch 1 micron. In same system again the etching was tried with the polysilicon recipe but the result was unsuccessful.

After that the etching of 1 micron oxide was tried in AMAT etch centura for 12 minutes in break and the recipe used was

Bias power=80 watts

Source power=800 watts

CF4=100 sccm

CHF3=10sccm

Pressure=15 m torr

The etching rate was confirmed in Ellipsometry and found that the 1 micron oxide etched completely.

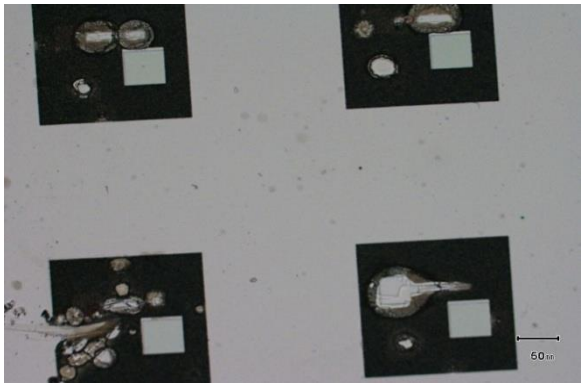


Fig.26. 2^{nd} level anchor patterning after dry etching in AMAT ETCH

6) Deposition of 1 micron polysilicon for anchor creation

Recipe used is as follows:

Base pressure=1.0e-6

Gas pressure=7.9e-1

Substrate temperature=300degree celsius

Filament temperature=1850 degree celsius

Ratio of gases SiH4:B2H6:H2=1:5:10, Voltage=26.1 Volts

Initially dummy run was taken and the thickness was verified in Cross SEM which was observed to be 1 micron as shown in Fig. 27.

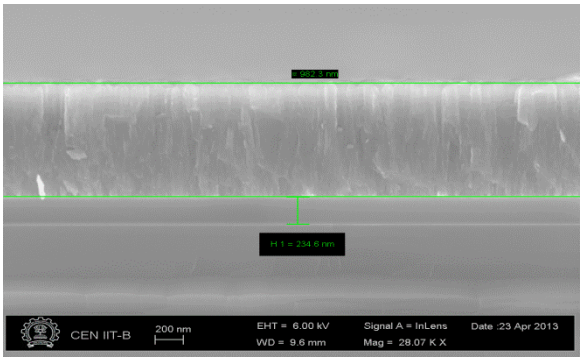


Fig.27.Cross SEM Images of polysilicon of thickness 230nm

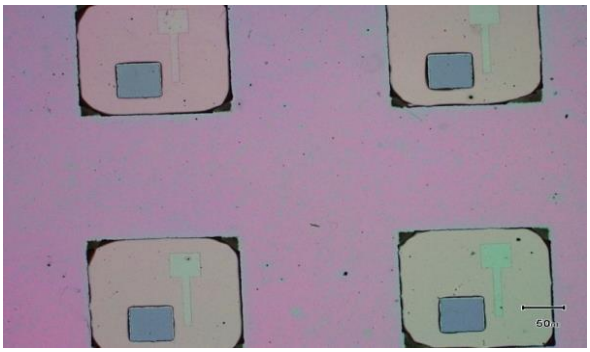


Fig.28.Olympus Image after 1 micron polysilicon deposition

3rd level masking was done after deposition of 1 micron polysilicon. While doing 3rd level masking the anchor post covered with PPR and the remaining was uncovered and as soon as it exposed to U.V light, it gets softened and developed with MF 319. DRY etching was done for etching 1 micron polysilicon using same recipe for 1 minute 45 seconds.

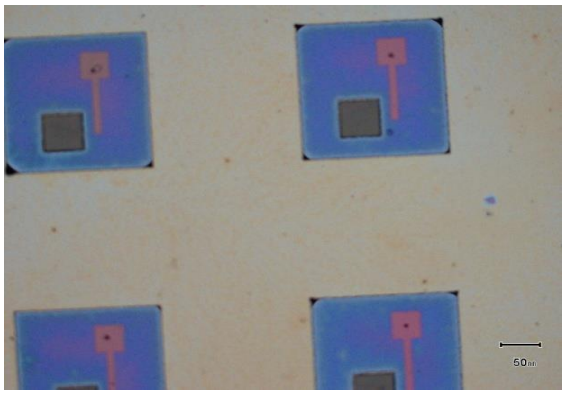
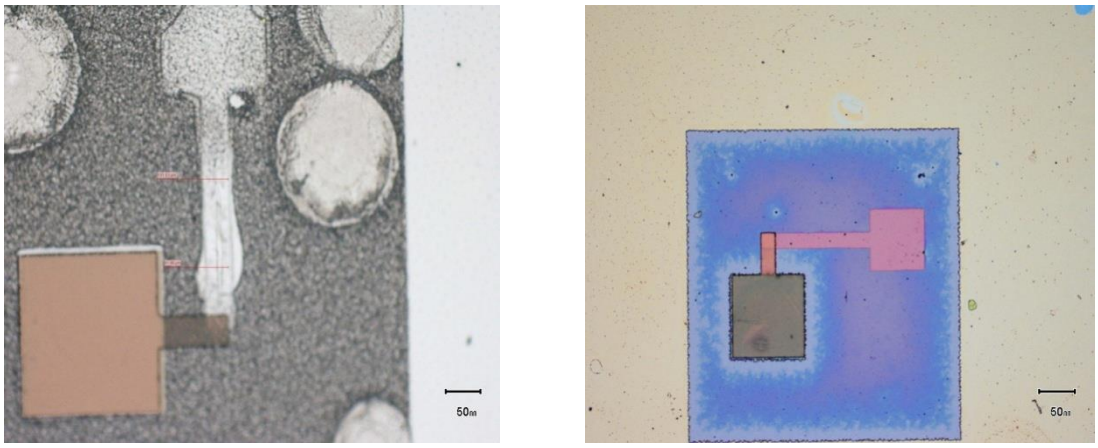


Fig.29. Olympus Image after 3rd level masking

7) 4th level exposure followed by immediate 3rd level Polysilicon deposition and 4th level patterning was done to transfer a beam structure to layer through mask and etching as shown below:



a) 4th level masking for beam with PPR b) 4th level masking for beam

Fig.30. Images for 4th level lithography for beam

8) The fabricated device was released by removing the sacrificial layer i.e oxide with BHF 5:1. While releasing the cantilever, colour change was observed. Also, to verify the etching results, contact angle measurement of the sample was done. In contact angle measurement angle was found to be greater than 90 degrees which means hydrophobic in nature i.e Sio_2 is removed completely otherwise it would be hydrophilic. Fig. 31. shows the image of released polysilicon cantilever. In Fig. 31. we can clearly see the gap between top beam and bottom electrode.

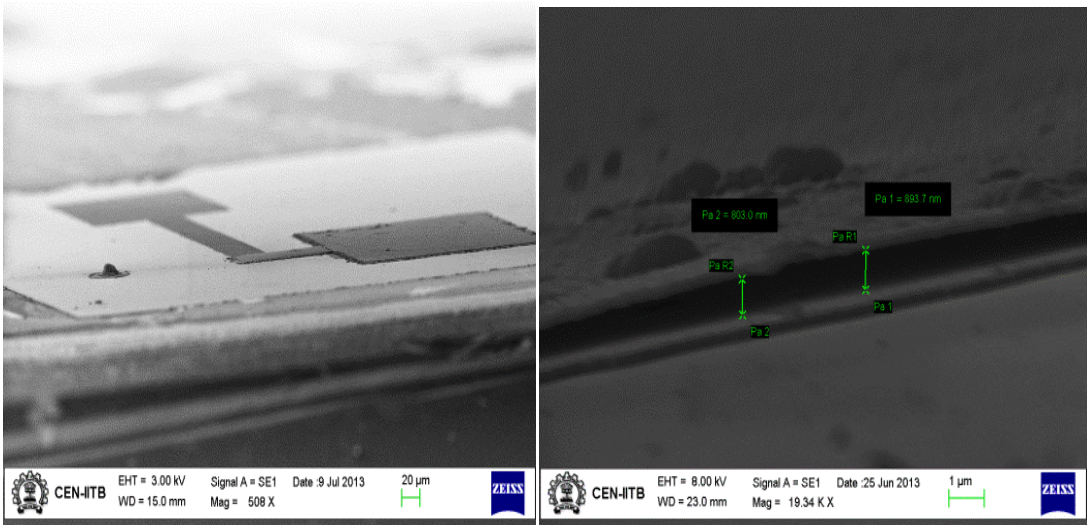


Fig.31. SEM Images of released polysilicon cantilever

3.3 Fabrication of Bi-layer Cantilever

Above polysilicon a layer of chrome-gold of thickness 10nm:100nm was deposited. Chrome was used for adhesion of gold and polysilicon layer. Thermal evaporator was used for deposition of chrome-gold. 5th level of Gold patterning was done to create a structural layer of polysilicon and gold as shown in Fig. 32.

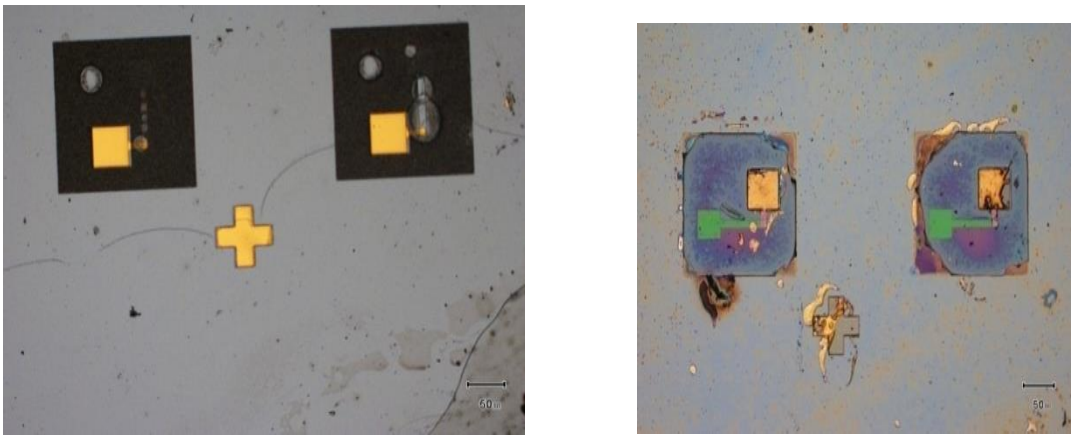


Fig 32. 5th level masking of gold layer

Gold layer was etched with wet etching in gold etchant a solution of KI (potassium iodide) ,then it was kept in chrome etchant for 1 minute. Finally the sacrificial layer i.e. oxide was removed with BHF 5:1. SEM images of bi-layer cantilever are shown in Fig.33.

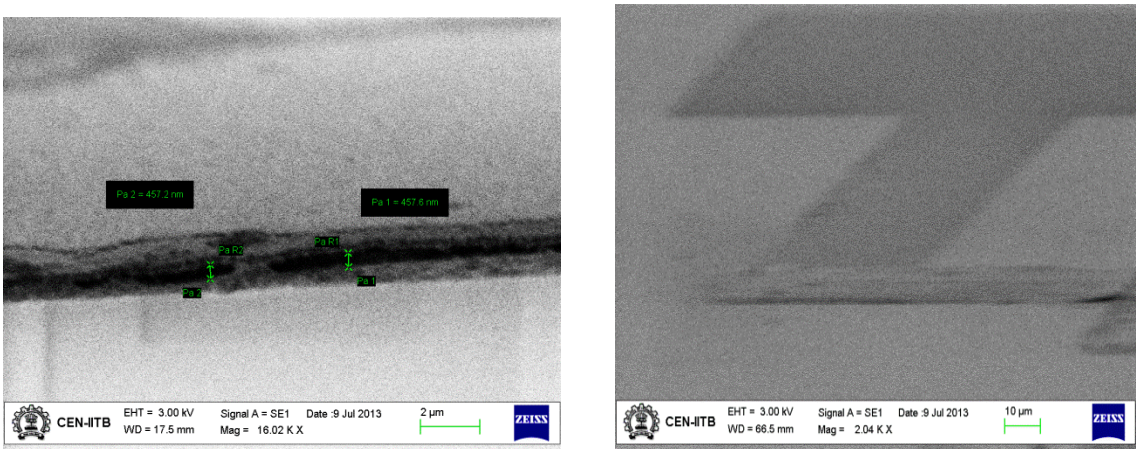


Fig.33. SEM images of released Bi-layer (polysilicon-gold) cantilevers

4. Electrical characterization

Electrical characterization experiments are performed on the fabricated device. Various experiments performed on these devices to validate the proposed methodology of this work. Use of microcantilever for temperature detection application is explored. The block diagram of characterization setup is shown in Fig.34.

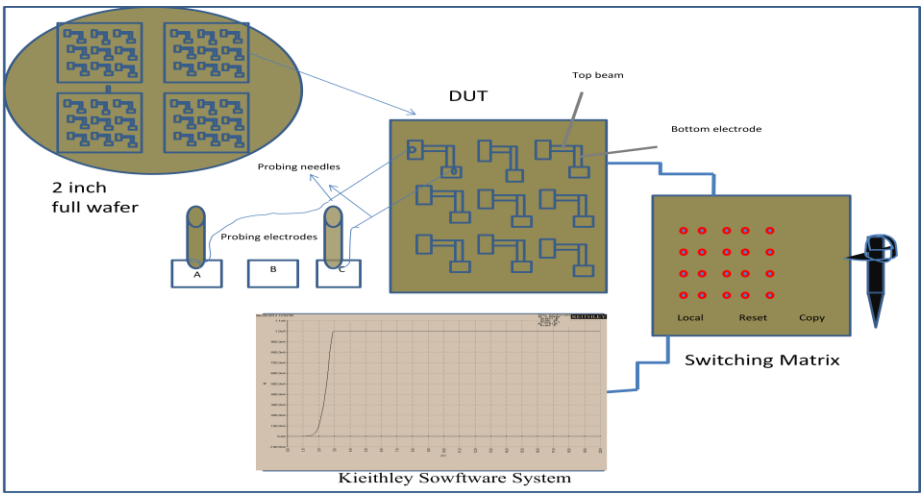


Fig. 34. Block diagram of Characterization set up

Electrical characterization set up used for testing and measurement of microcantilever is shown in Fig.35.

Fig. 35. Electrical characterization setup

Electrical characterization set up used for testing and measurement of microcantilever is shown in Fig.35. Electrical characterization system consist of Karl Suss shielded probe station, Switching Matrix and Keithleys 4200 Semiconductor Characterization System (4200 SCS).

- Karl Suss shielded probe station: provides the isolation of EMI effect and provide a point contact to the devices using probing needle.
- Switching Matrix : It provides the multiple connecting switches. It connects input and output from probe station to the Keithleys 4200SCS.
- Keithleys 4200 SCS: It offers Precision DC Current-Voltage (I-V) measurements and other measurements which are the foundations of a full characterization plan.

4.1 Current-Voltage (I-V) Characterization

The Current-Voltage (I-V) measurement is the basic tool for electrical characterization of microcantilever. Using this method pull-in voltage is evaluated. The applied voltage was swept from 0 volt to 4 volt between bottom electrode & top cantilever and current was measured. The current shoots up at pull-in voltage of 2.35Volt shown in Fig.36. From the Fig.36, it can be seen that the cantilever is showing a switching action which is due to the electrostatic actuation at 2.35 Volt. This is defined as pull-in voltage for the cantilever. The current passes through the device as cantilever and bottom electrode is in contact at 2.35 volt. Compliance value is given for the safety of device operation, to avoid breakdown or permanent failure of the device. Hence the preset voltage for the cantilever device will be less than 2.35 volt. This is required for temperature detection application.

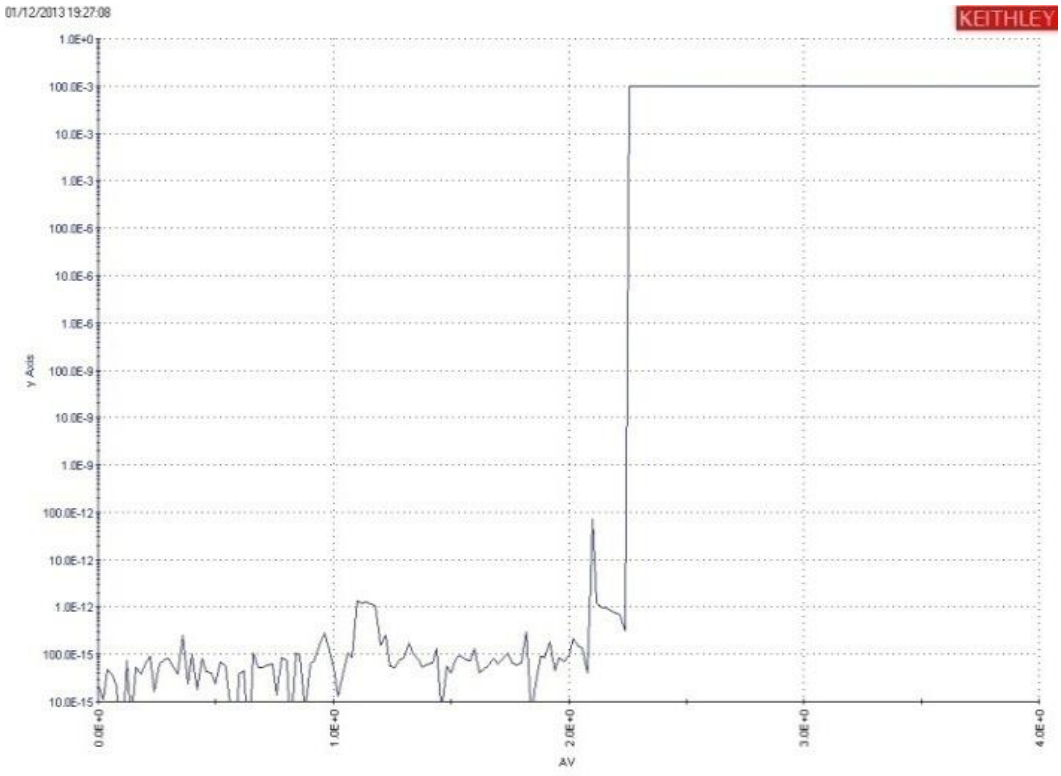


Fig.36. I-V characterization fabricated device.

4.2 Experiments for temperature detection

This characterization is done to demonstrate the use of microcantilever for temperature detection. In this, the experimental analysis such as effect of temperature on the cantilever device without application of electrostatic force (potential) is analyzed. It was found that it took a very high temperature (more than 200^0 C) for causing the deflection of 1 micron of cantilever beam. Hence the concept of prestressing comes to the picture. An electrostatic force is used to predeflect the cantilever by applying potential across the top and bottom electrode (contact). With preset voltage a desired gap can be achieved and a particular temperature can be detected shown in Fig. 37.

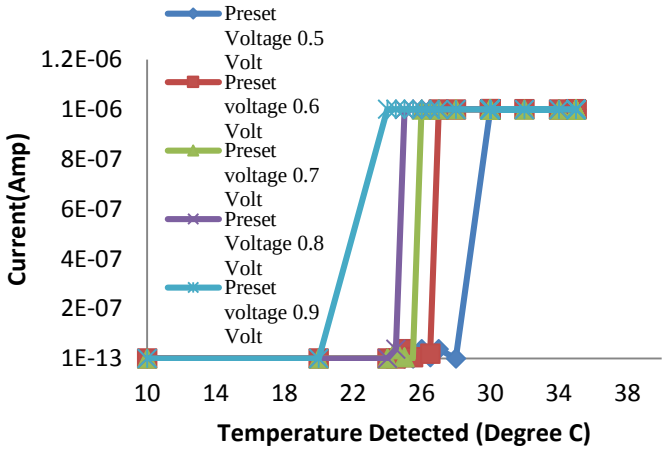


Fig.37. Experimental results for detection of set temperature with preset voltage

4.3 Transient Analysis of Microcantilever Based Sensor

An experiment was also done to understand the transient characteristics of cantilever. The devices operate at the operating or pull in potential of 2-2.5 volt. Hence the pulse amplitude is kept at 2.5 volt and pulse width is varied from 10 ns to 500 ns. We have applied pulse from external Pulse Generator Unit and provided to the fabricated device. The response of the device under test (DUT) is then captured using Digital Storage Oscilloscope (DSO). Block diagram and Experimental set up used for pulse characterization is shown in Fig.38 and Fig. 39 respectively.

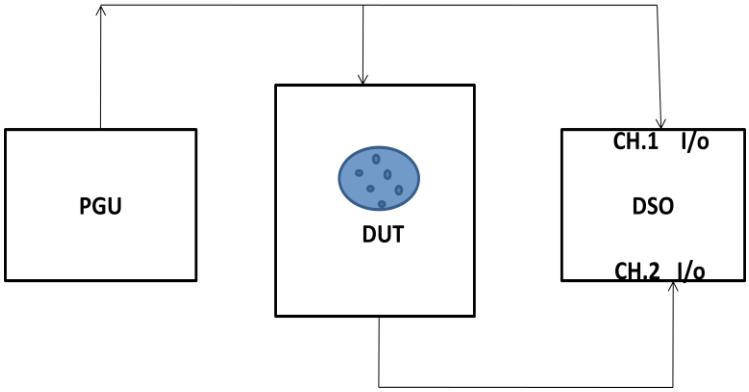


Fig.38. Block diagram pulse characterization setup

In this experimental set up we used external PGU (Pulse Generation Unit) of Agilent B818A, probe station unit of Karl Suss and external DSO for measuring as well as capturing the output response.

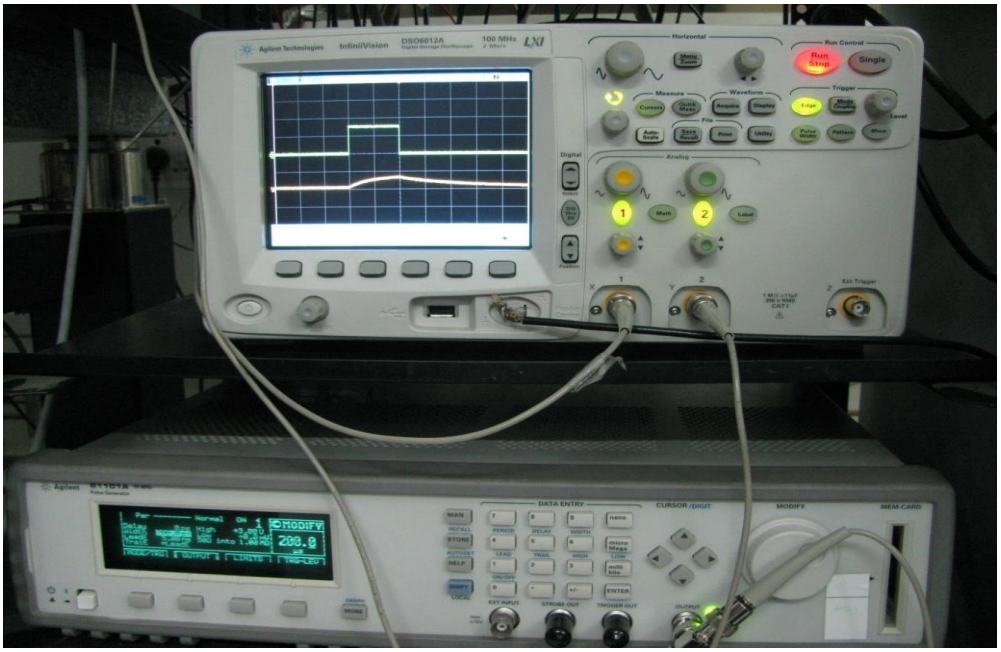


Fig. 39 experimental set up we used for pulse characterization

When pulse width was varied from 10 ns to 60 ns, we observed that output does not follow the input as sensor requires more time to respond. Output is 0 volt at all the time. When 2.5 volt 100 ns pulse was applied response of the device obtained is shown in Fig.40.

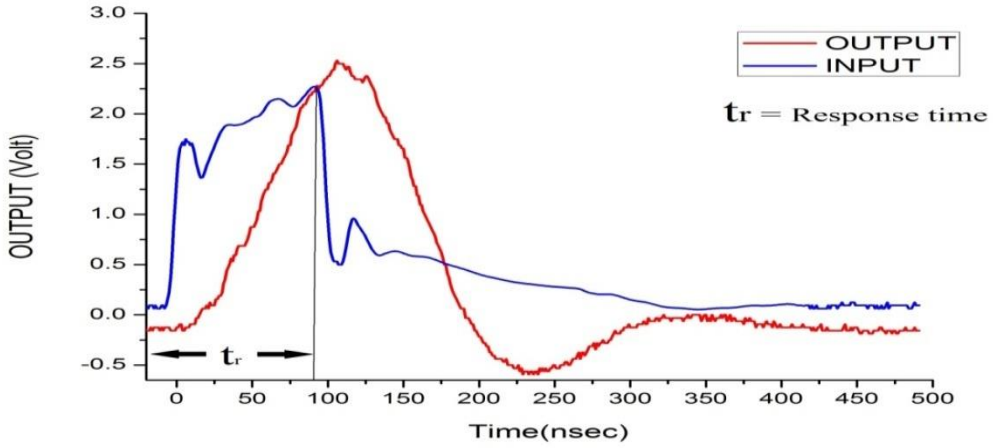


Fig.40. Response of sensor for 2.5Volt 100 nsec pulse

From these studies we can conclude that sensor is taking approximately 90 ns to respond to the external stimulus.

4.4 Experimental Results for single layer and bi-layer cantilevers

Similar experiment discussed earlier for aluminium cantilevers, was performed for single layer polysilicon and bi-layer microcantilevers. Experimental results are shown in Fig.41-44.

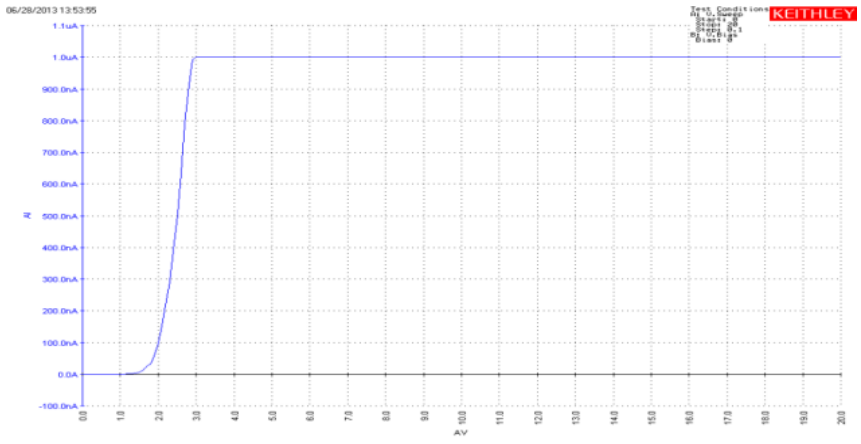


Fig.41. I-V Characterization of single layer

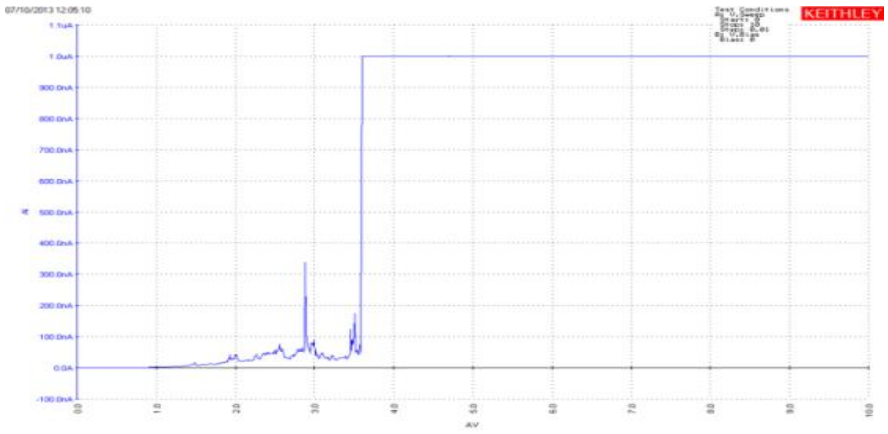


Fig.42. I-V Characterization of Bi-layer Structure

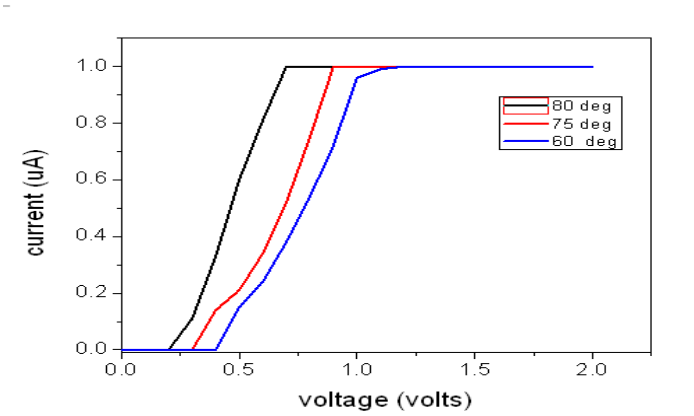


Fig.43. Temperature dependent I-V Characterization of single layer structure

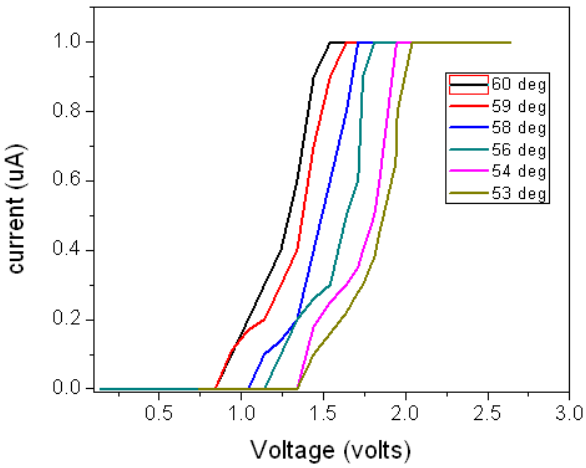


Fig.44. Temperature dependent I-V Characterization of bi-layer structure

Experiments were done on bi-layer cantilevers (poly-gold) cantilever for the detection temperature with preset voltage. The experimental results are shown in Fig.45.

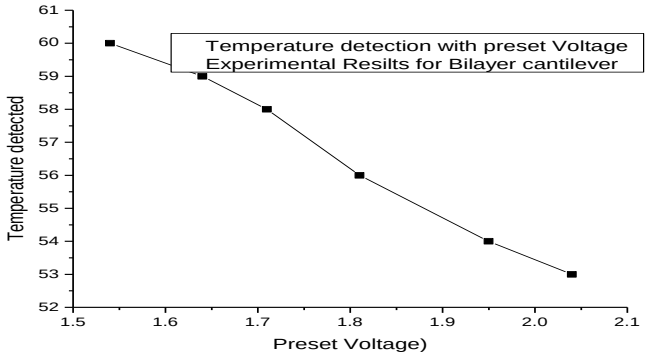


Fig.45. Temperature detected by poly-gold cantilevers at various preset voltage levels

Transient characteristics of cantilever are observed using the same procedure discussed earlier. The devices pull in potential is 3 volt-3.2 volt for single layer microcantilever. Bi-layer devices operate at the operating or pull in potential of 3.6- 3.9V. The pulse is varied from nanoseconds to microseconds to observe the response of the device. From the pulse characterization results of single layer and bi-layer cantilever devices, it can be concluded that response time for voltage stimuli for bi-layer cantilever device is 2 μs which is less than that of single layer 5 μs.

5. Conclusion

Knowing the importance of sensors in present world many new sensors are being investigated. In this work microcantilever sensors with electrical readout method has been designed and developed. Metal, polysilicon and bi-metal cantilevers with surface micromachining were fabricated. The processes for fabrication with five step lithography were developed for each of these microcantilevers. Electrical characterization of these microcantilevers was performed. The device was prestressed with the voltage and different temperatures could be detected. Experimental results are validating the use of the microcantilever for temperature detection. The operating range for temperature sensing application is improved in bi-layer structure which is experimentally demonstrated. The experiment was also done to understand the transient characteristics of cantilever. The fabricated device can be used for temperature control application. These measurements probably are useful in other sensors such as biosensor and accelerometer development.

References

[1] Anja Boisen, Søren Dohn, Stephan Sylvest Keller, Silvan Schmid and Maria Tenje, "Cantilever-like micromechanical sensors" Rep. Prog. Phys. 74(2011) 036101, pp 30

[2] L.G. Carrascosa and M. Moreno, "Nanomechanical biosensors : a new sensing tool," Trends Anal. Chem., vol. 25, 2005, pp. 196–206.

[3] C.A. Savran, T.P. Burg, J. Fritz, and S.R. Manalis, "Microfabricated mechanical biosensor with inherently differential readout," Applied Physics Letters, vol. 83, 2003, pp. 1659-1661.

[4] B. N, B. J, de R.N. F, and D. U, "Scanning force microscopy in the dynamic mode using microfabricated capacitive sensors," J. Vac. Sci. Technol. B, vol. 14, 1996, pp. 901.

[5] A.A. Barlian, W.-tae Park, J.R.M. Jr, A.J. Rastegar, B.L. Pruitt, and M. Engineering,"Review: Semiconductor Piezoresistance for Microsystems," Proc IEEE Inst Electron Eng, vol. 97, 2009, pp. 513-552.

[6] C.-H. Chen1, R.-Z. Hwang1, L.-S. Huang1, S. Lin1, H.-C. Chen1, Y.-C. Yang1,Y.-T. Lin1, S.-A. Yu1, Y.-H. Wang2, N.-K. Chou2, S.-S. Lu1"A Wireless Bio- MEMS Sensor for C-Reactive Protein Detection Based on Nanomechanics", ISSCC 2006 / Session 30 / Silicon for Biology / 30.6, IEEE International Solid-State Circuits Conference

[7] N P Mahalik, "MEMS", Department of Industrial Technology, California state university, California.

[8] Gary S. May, Simon M. Sze , "Fundamentas of semiconductor Fabrication," John Wiley & Sons, INC.

[9] Saurab K. Ghandhi "VLSI Fabrication Principles," Second Edition, , A Wiley-Interscience Publication, John Wiley & Sons, INC.

[10] http://www.inup-iitb.org/facilities

Acknowledgement

We are thankful to Center For Excellence In Nanoelectronics and Nanoelectronics Device Charcterization Laboratory (IITB, Powai, Mumbai) for making this project a reality. We thank IITB for all the technical and non-technical support. Our Sincere acknowledgement to Chief investigators of INUP Programme Prof. V. Ramgopal Rao and Prof. A. Q. Contractor and Co-Chief investigators Prof. J. Vasi and Prof. Anil Kottantharavil. We also thank Dr. Nageswari, for providing their whole hearted and unending support during the fabrication and Characterization processes.

We hereby thank Director and Head of the Electronics Engineering Department ,VNIT, Nagpur for the support. We also acknowledge Staff members and researcher of National MEMS Design Centre and Electrical Characterization laboratory, VNIT, Nagpur for the support.

We also thank Principal and management of RCOEM, Nagpur for permitting us to carry out the project work and providing their help and support during this project. We would like to thank Head of the Electronics Engineering Department and M. Tech Coordinator for all kinds of cooperation and support.

We also acknowledge our PG students, Mr. Aditya Dhanvijay and Ms. Priya Borkar for providing the support for fabrication and characterization work in this project. .